HHW Industrial microSD Card

SD3.0

Datasheet

Rev. 1.0

杭州瀚海微科技有限公司
www.hanhai-tech.com

杭州瀚海微科技有限公司
www.hanhai-tech.com

杭州瀚海微科技有限公司
www.hanhai-tech.com

3. Specifications

3.1. Performance

Max. Data Transfer Rate

- Read: 120MB/s; Write: 70MB/s

3.2. NAND Flash Memory

Industrial microSD Card uses TLC NAND Flash memory, which is non-volatility, high reliability and high speed memory storage.

3.3. Power Requirement

3.3.1. DC Input Voltage

杭州瀚海微科技有限公司
www.hanhai-tech.com

杭州瀚海微科技有限公司
www.hanhai-tech.com

4.2.3 Bus Signal Line Load

Table 7: Bus Operating Conditions - Signal Line's Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	KΩ	To prevent bus floating
Total bus capacitance for each signal line					

杭州瀚海微科技有限公司
www.hanhai-tech.com

4.2.5 Bus Timing (Default)

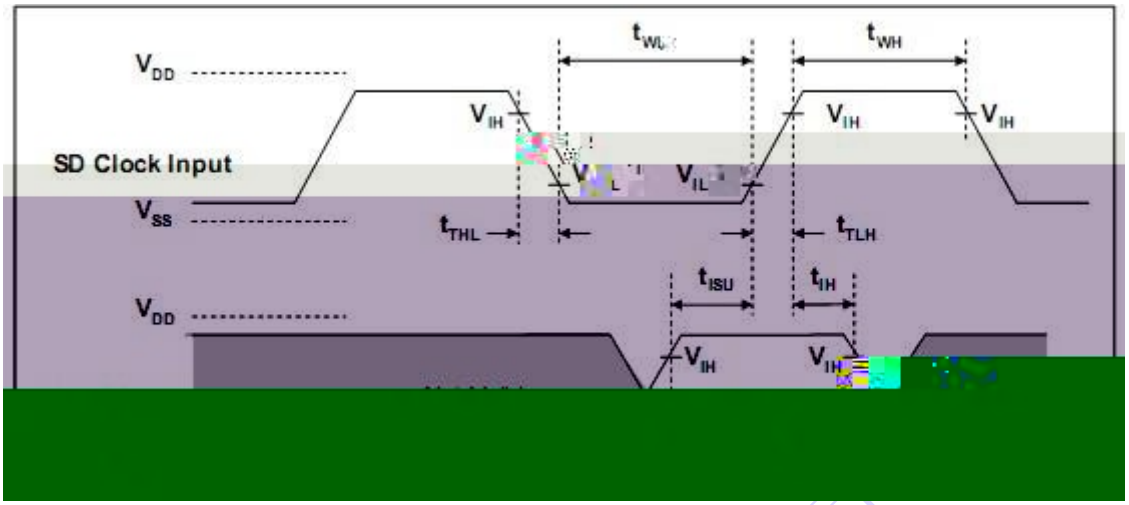


Figure 3: Card input Timing (Default Speed Card)

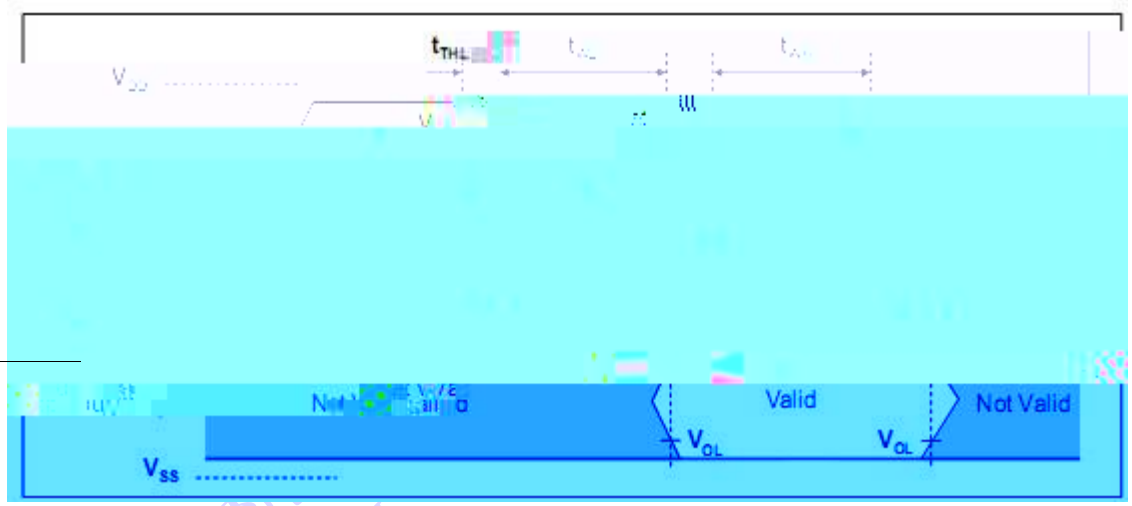


Figure 4: Card Output Timing (Default Speed Mode) Table 8: Bus Timing-Parameters Values

Parameter (Default Speed)	Symbol	Min.	Max	Unit	Remark
Clock CLK All values are referred to min V_{IH} and max V_{IL}					
Clock frequency data transfer	fpp	0	25	MHz	$C_{CARD} \leq 10pF$ (1 card)
Clock frequency Identification	f_{OD}	0[(1)]/100	400	KHz	$C_{CARD} \leq 10pF$ (1 card)
Clock low time	t_{WL}	10		ns	$C_{CARD} \leq 10pF$ (1 card)
Clock high time	t_{WH}	10		ns	$C_{CARD} \leq 10pF$ (1 card)
Clock rise time	t_{TLH}		10	ns	$C_{CARD} \leq 10pF$ (1 card)
Clock fall time	t_{THL}		10	ns	$C_{CARD} \leq 10pF$ (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5			

Input hold time	t_{TH}	5		ns	C_{CARD} ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≤ 40pF (1 card)
Output Hold time	t_{OH}	0	50	ns	C_L ≤ 40pF (1 card)

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required (refer to Chapter 4.4-Clock Control)

4.2.6 Bus Timing (High-Speed Mode)

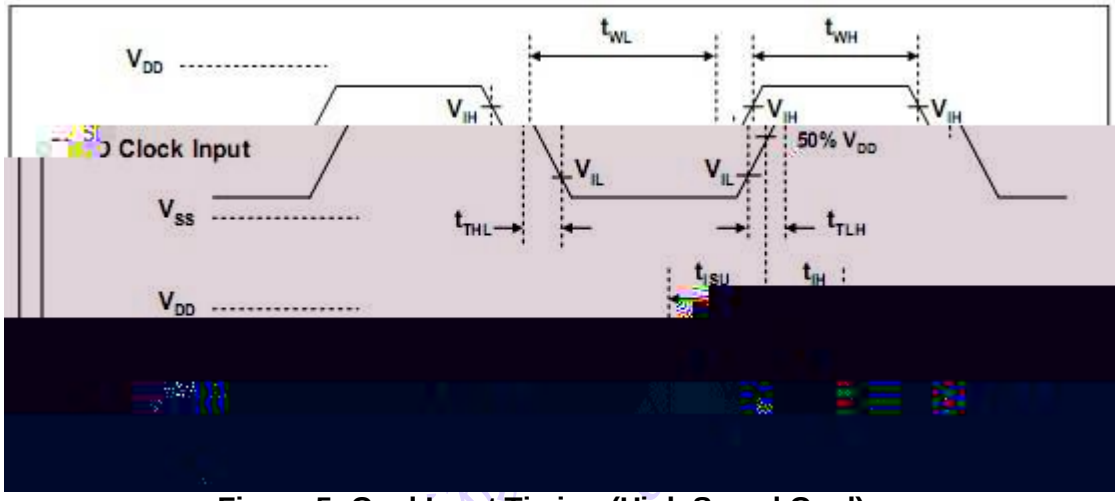


Figure 5: Card Input Timing (High Speed Card)

杭州瀚海微 www.hanhai

Figure6: Card Output Timing (High Speed Mode)

Table 9 : Bus Timing – Parameters Values(High Speed)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK All values are referred to min V_{IH} and max V_{IL}					
Clock frequency data transfer	fpp	0	50	MHz	C_{CARD} ≤ 10pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} ≤ 10pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} ≤ 10pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} ≤ 10pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} ≤ 10pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{TH}	2		ns	C_{CARD} ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40pF (1 card)
Output Hold time	t_{OH}	2.5		ns	C_L ≥ 15pF (1 card)
Total System capacitance for each line[1]	C_L		40	pF	1 card

1) In order to satisfy sever timing, host shall drive only one card.

4.3 Bus Operation Conditions for 1.8V Signaling

4.3.1 Threshold Level for High Voltage Range

Table 10: Threshold Level for High Voltage

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4		V	I_{OH}=2mA $V_{DD\ min}$
Output Low Voltage	V_{OL}		0.45	V	I_{OL}

4.3.3 Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

4.3.3.1 Clock Timing

Figure 7: Clock Signal

Timing Table 12: Clock

Signal Timing

海微科技有限公司
ai-tech.com

4.3.3.2 Card Input Timing

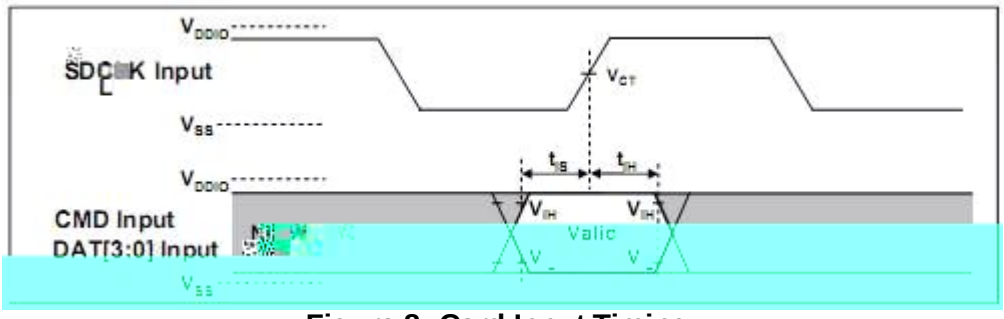


Figure 8: Card Input Timing

Table 13: SDR50 and SDR104 Input Timing

Symbol	Min	Max	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD}

4.3.3.3 Card Output Timing

4.3.3.3.1 Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

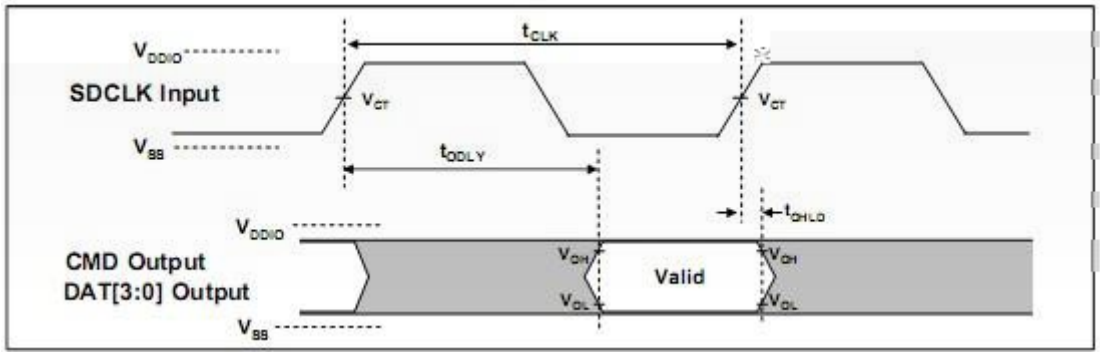


Figure 9: Output Timing of Fixed Date

Window Table 14: Output Timing of Fixed

Data Window

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, CL=30pF, using driver Type B, for SDR50.
t_{ODLY}		14	ns	t_{CLK} ≥20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). CL=15pF

4.3.3.3.2 Output Timing of Variable Window (SDR104)

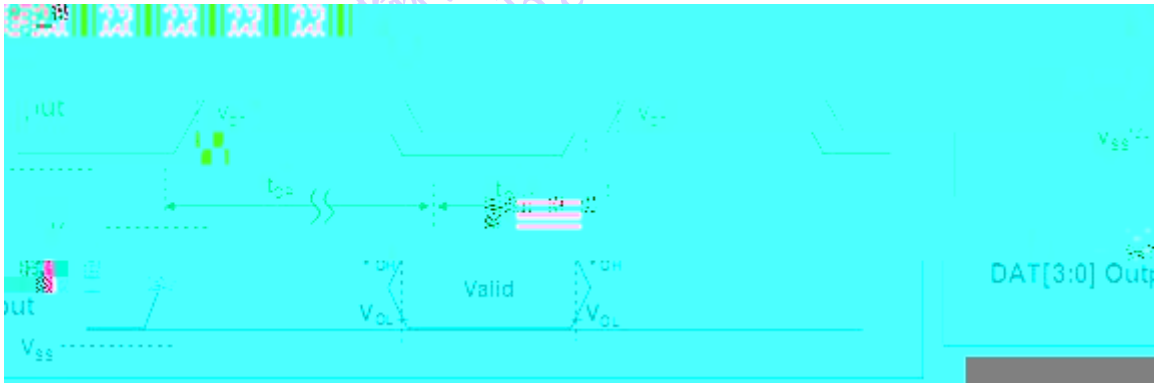


Figure 10: Output Timing of Variable Data

Window Table 15: Output Timing of Variable

Data Window

Symbol	Min	Max	Unit	Remark
t_{OP}	-	2	UI	Card Output Phase
t_{OP}	-350	+350	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

5. Mechanical Dimensions

The mechanical dimensions of Agrade Industrial microSD Card were basically followed the mechanical form factor definitions on microSD card specifications which constructed by SD card association.

Figure 11: Top View
Figure 12: Side View

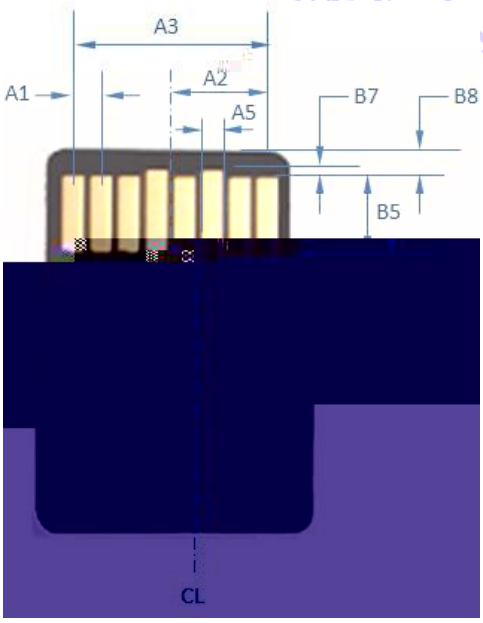


Figure 13: Bottom View

6. Ordering Information

	microSD Card(SLC)	microSD Card(TLC)
Capacity	Wide-temperature	Wide-temperature
1GB		HHW256GTFT-33
2GB	HHW2GTFS-33	
4GB	HHW4GTFS-33	