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SD NAND SPECIFICATION

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1. Overview

1.1 Product Description

Hanhai-tech SD NAND are highly integrated flash memories with serial and random access capability. Can be use in the device which can support SD2.0 standard. It is accessible via a dedicated serial interface optimized for fast and reliable data transmission.

The purpose of product development is to make memory chips based on SD interface more stable and use scenarios more abundant. Han hai-tech SD NAND can match more MCUS with stable quality and strong compatibility, and can perfectly replace the previous storage products based on SDIO interface. The low power consumption of the product itself is more suitable for handheld products, and the rigorous production process makes the product more suitable for diverse scenarios

1.2 Features Summary

-Capacity: 1GB
-Complies to SD Specification V2.0
-Supports SD SPI Mode
-Voltage range for communication: 2.7~3.6V
-Variable clock rate 0-25 MHz (standard), 0-50 MHz (high performance)
-Up to 25 MB/sec data transfer rate (using four paralleCte-6.6 (a)0(c)-26 (to)-0.9 (,)-
u2

ignment

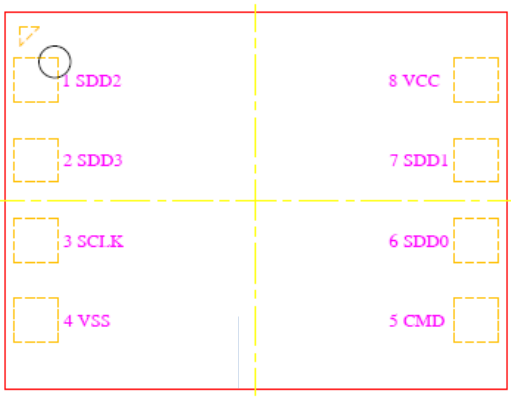


Figure 1:Top View

SD Mode		SPI Mode	
e	Description	Tyte	Description
PP	Data Line [Bit2]	RSV	Reserved
PP	Data Line [Bit3]	I3	Chip select(neg true)
	Clock	I	Clock
	Supply voltage ground	S	Supply voltage ground
	Supply voltage	S	Supply voltage
PP	Data Line [Bit1]	RSV	Reserved
PP	Data Line [Bit0]	OPP	Data Out

3. Product List

Product model	Capacity	Actual Size	Sequential R/W (Note1)	Package
[redacted] S66I-A1				

6. Physical Dimension



Figure 2:Top View and Side View

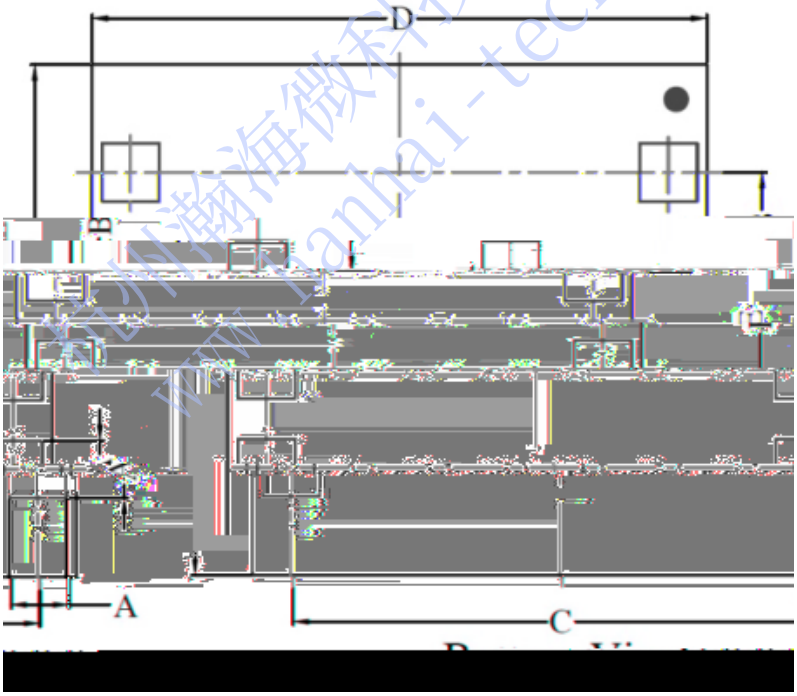
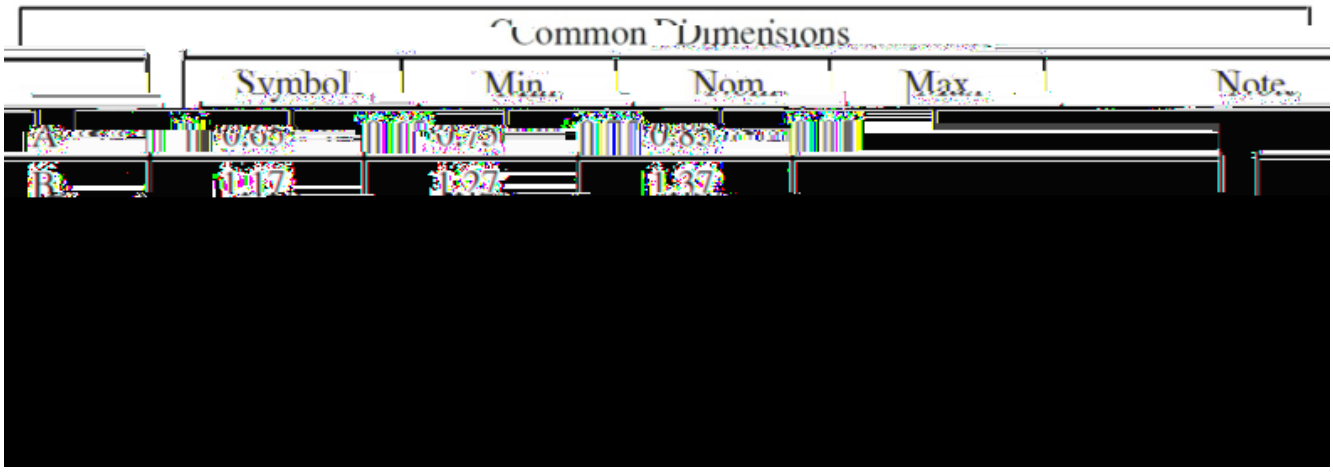


Figure 3: Bottom View

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7. Recommended Schematic

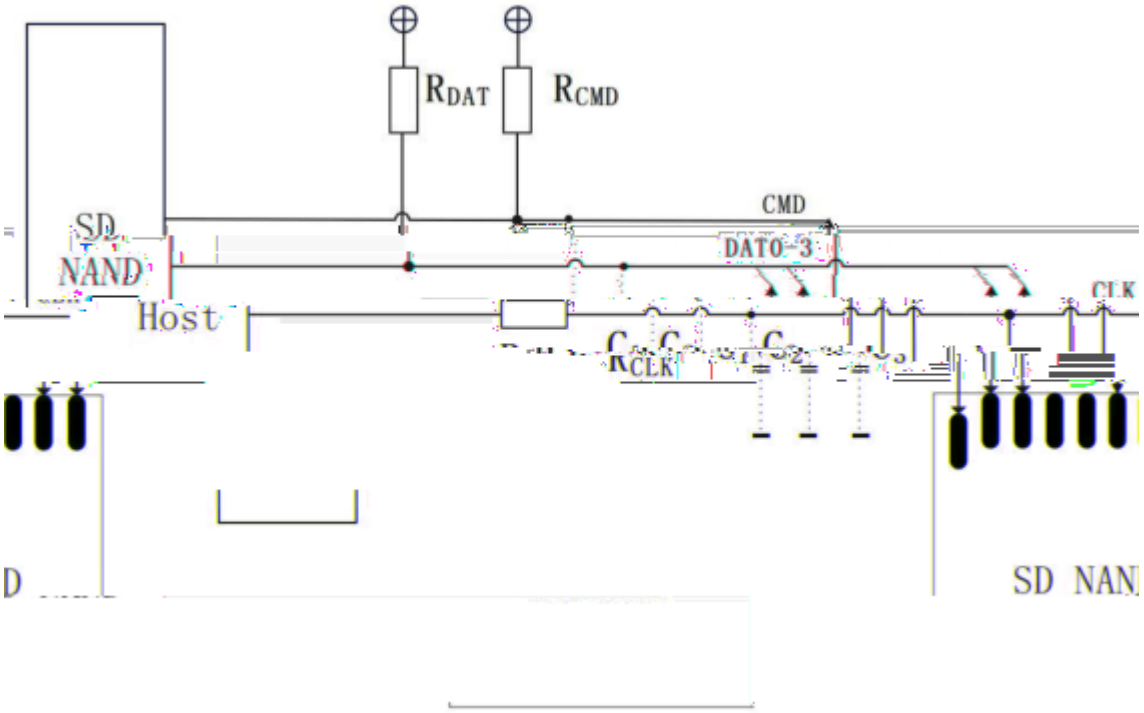


Figure 4: Recommended Schemati

Note:

Rdat and Rcmd (10K-100kΩ) are pull-up resistors protecting the CMD and the DAT lines against bus floating when SDNAND is in a high-ll-

simultaneously - Since there is no Open Drain mode in SD Memory Card, this type of command shall be used on

e-0.017 Tc 0.017 Tw 0.348 0 Td[(te)-26.2 (c)-38.7 (h)17.2 (

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
		basic	reserved	block read	reserved	write block, erase	write protection	lock card.	application specific	I/O mode	switch	reserved	
0	Mandatory	+											CMD
2	Mandatory	+											CMD
3	Mandatory	+											CMD
4	Mandatory	+											CMD
5	Optional									+			CMD
6[2]	Mandatory										+		CMD
									CMD7		Mandatory		+
									CMD8[3]		Mandatory		+
									CMD9		Mandatory		+
									CMD10		Mandatory		+
									CMD11[5]		Optional		+
									CMD12		Mandatory		+

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CMD56	Mandatory									+			
CMD57[2]	Optional											+	
ACMD6	Mandatory									+			
ACMD13	Mandatory									+			

9. Write Performance

Below table shows the typical data management of the card when the host writes RUs of an AU. When

(1) Read Performance of Stream Data

11. SPI Mode

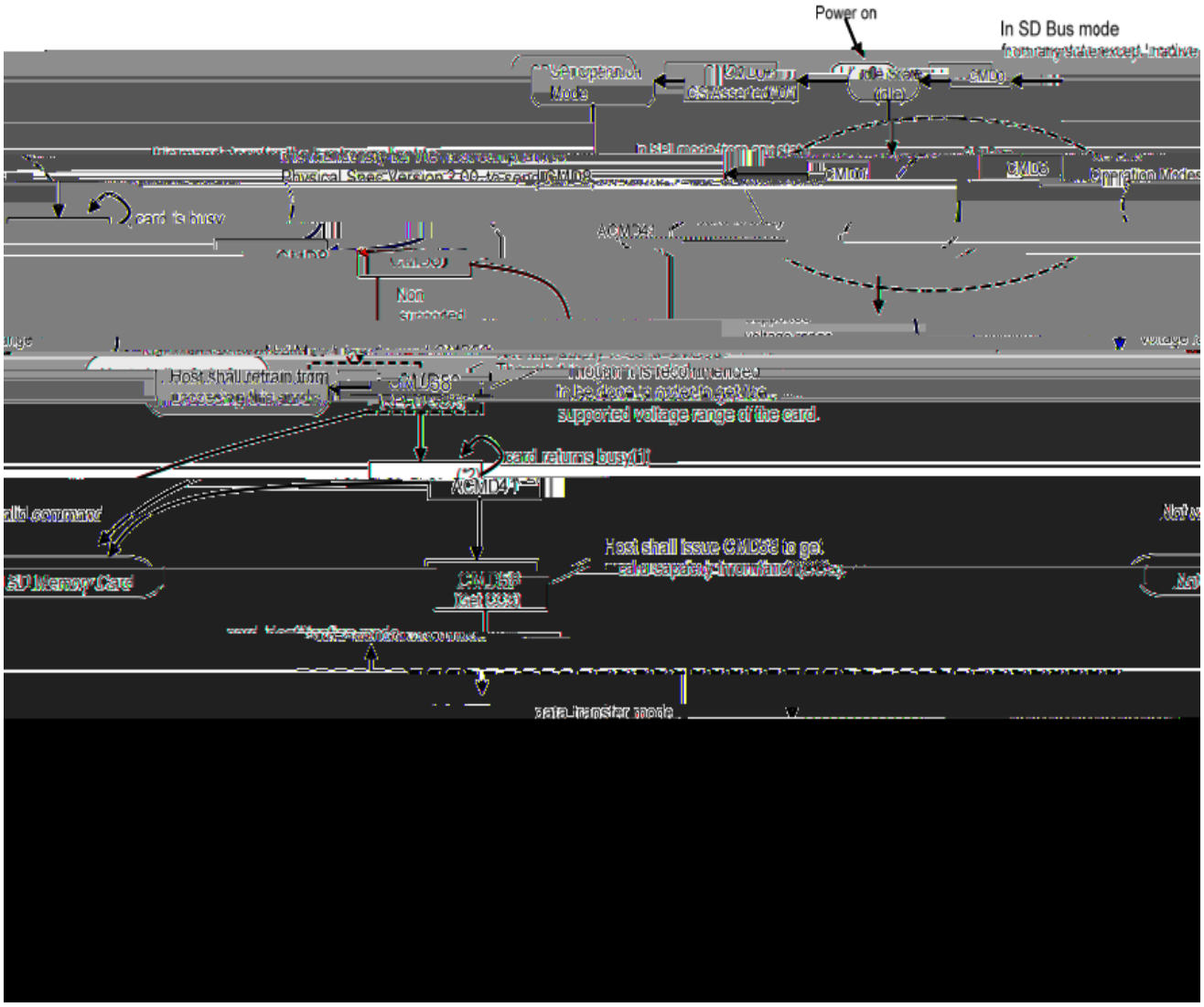
The SPI mode consists of a secondary communication protocol that is offered by Flash-based SD Memory Cards. This mode is a subset of the SD Memory Card protocol, designed to communicate with a SPI channel, commonly found in Motorola's (and lately a few other vendors') micro controllers. The interface is selected during the first reset command after power up (CMD0) and cannot be changed once the part is powered on.

The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses a subset of the SD Memory Card protocol and command set.

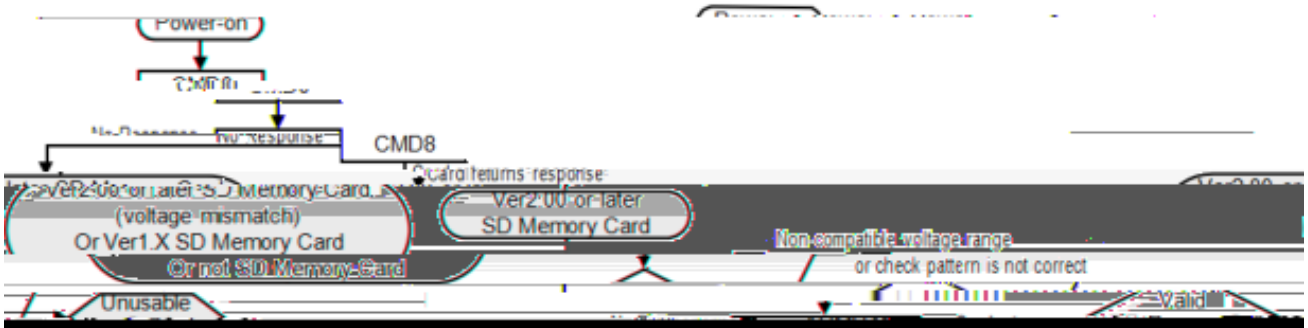
The advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance of the SPI mode versus SD mode (e.g. Single data line and hardware CS signal per card).

The commands and functions in SD mode defined after the Version 2.00 are not supported in SPI mode. The card may respond to the commands and functions even if the card is in SPI mode but host should not use them in SPI mode.

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Power on
In SD Bus mode
CMD0
Inactive
Idle State
(Idle)
CMD0
CS Asserted (CD3)
CMD8
Physical Spec Version 2.00 /ACMD41
CMD55
ACMD41
Non
supported
Host shall refrain from
accessing the card
CMD58
Host shall issue CMD58 to get
OCR register
card returns busy(0)
ACMD41
Host shall issue CMD58 to get
OCR register
SD Memory Card
CMD2
Get CID
Data transfer mode

12. SD Mode

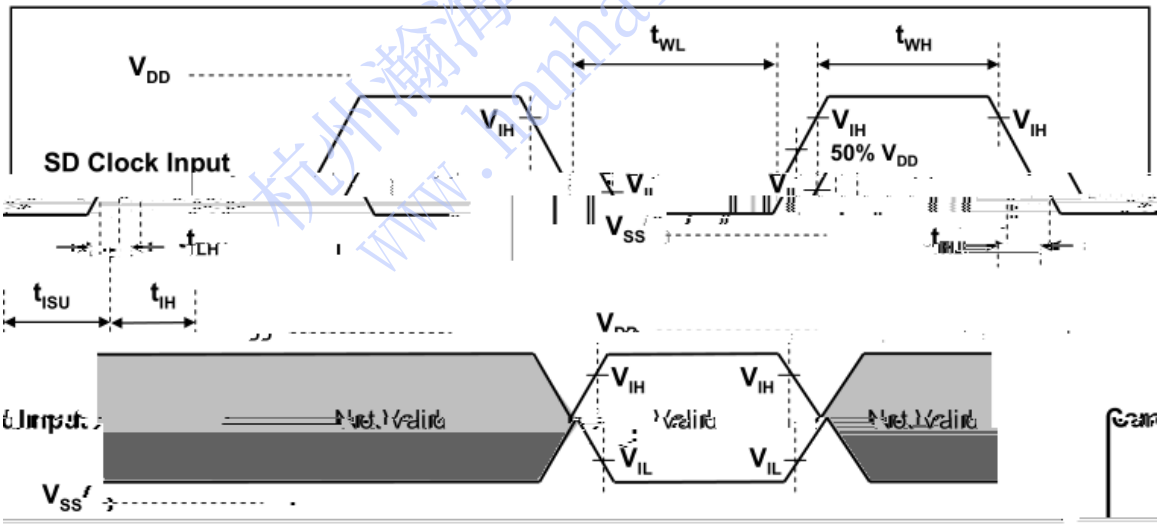


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13. DC Characteristics

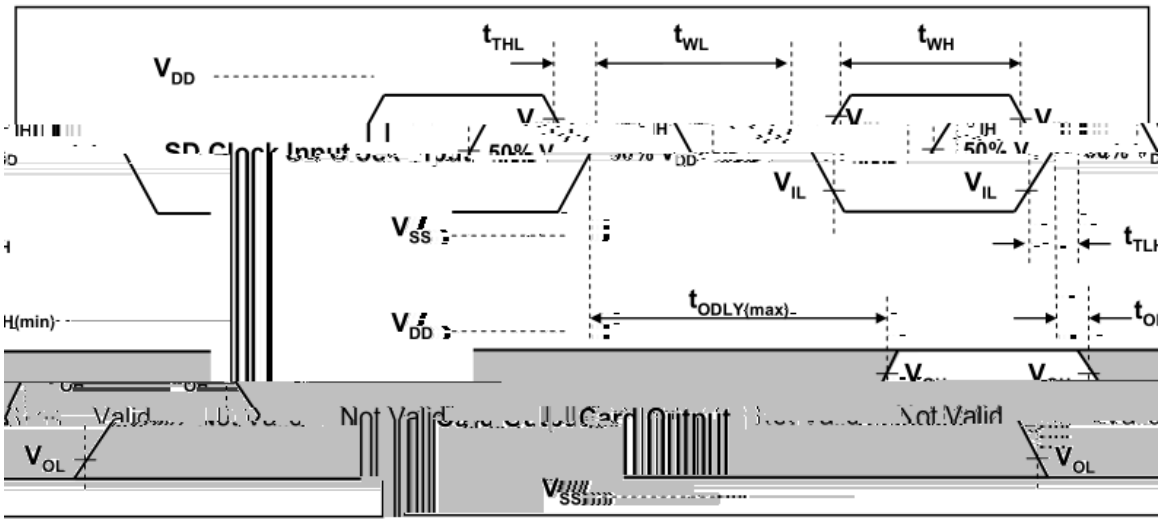
Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low voltage		VSS-0.3		0.25VCC	V
V_{IH}	Input high voltage		0.625VCC		VCC+0.3	V
V_{OL}	Output low voltage	IOL=100μA @VCC_min			0.125VCC	V
	Output high voltage		0.75VCC		@vcc_min	
	Tristate output leakage current					
I_{STBY}	Standby current	3.3V@clock stop		150	200	μA
	Operation current	3.3v@50MHz (Write)	15	25	mA	I_{OP}
		(Read)	15	25	mA	

14. Bus Timing (High-Speed Mode)



Card Input Timing (High Speed Card)

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Card Output Timing (High Speed Mode)

15. Power Up



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Power-up Diagram

'Power up time' is defined as voltage rising time from 0 volt to Vop min (refer to 6.6) and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

'Supply ramp up time' provides the time that the power is built up to the operating level (Host Suppl Voltage) and the time to wait until the SD card can accept the first command.

The host shall supply power to the card so that the voltage is reached to Vdd min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPl mode, CS shall be held to high during 74 clock cycles.

After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the idle state. ln case of SD host, CMDO is not necessary. ln case of SPl host, CMDO shall be the first command to send the card to SPI mode.

CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 or later host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.

ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up seauence, In case the host system connects multiple cards the host shall checkm thca-2.6 (st)18.2 ( )