Timing Values

Parameter	Min.	Max.	Unit	Remark
N_{CR}	2	64	clock cycles	Period between an end bit of command and a start bit of response except CMD2 and ACMD41.
N_{ID}	5	5	clock cycles	Period between an end bit of command and a start bit of response for CMD2 and ACMD41.
N_{AC}[1]	2		clock cycles	Period between an end bit of command and a start bit of
				read data a
n end bit of response and a start bit of	N_{RC}	8	clock cycles	Period between a next command.
n end bit of command (CMD0, CMD4, and a start bit of next command.	N_{CC}	8	clock cycles	Period between a CMD7 de-select)
n end bit of response and a start bit of	N_{WR}	2	clock cycles	Period between a

Timing Values (Except SDR50 and SDR104)

1) The maximum read access time for a Standard Capacity SD Memory Card shall be calculated by host as follows:

tAAC(max) = 100[ms] (TAAC = fpp) + (100[ms] NSAC)) ,

fpp is the interface clock rate and TAAC & NSAC are given in the CSD (Chapter 5.3).

Details of read, write, and erase timeouts are described in 4.6.2

In the case of SDHC and SDXC, a fixed value (100ms) shall be used for the maximum read access time.

Gap

CMD12

CMD12

ŋ